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09/829,161	04/09/2001	Salman Akram	3442.1US (96-428.1)	8260

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TRASK BRITT  
P.O. BOX 2550  
SALT LAKE CITY, UT 84110

EXAMINER

NGUYEN, HA T

ART UNIT

PAPER NUMBER

2812

DATE MAILED: 07/21/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

09/829,161

Applicant(s)

AKRAM, SALMAN

Examiner

Ha T. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 10 June 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-26, 72, 82 and 84-106 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-26, 72, 82 and 84-106 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

## **DETAILED ACTION**

### ***Notice to applicant***

1. Applicant's Amendment and Response to the Office Action mailed 3-21-3 and request for an RCE have been entered and made of record (Paper Nos. 18 and 20). Following is an Office Action responding to this request.

### ***Response to Amendment***

2. In view of Applicant's cancellation of the claim, the rejection of claim 83 under 35 U.S.C. 103 is rendered moot.

In view of Applicant's arguments amendment to the claims, the rejections of claims 72, 79, and 84 under 35 U.S.C. 102 or 103 as being anticipated by or unpatentable over Joo (USPN 5879957) have been withdrawn.

Applicant's arguments with regard to the rejections under 35 U.S.C. 103, as being unpatentable over Brown (USPN 6030896) have been fully considered, but they are not deemed to be persuasive for at least the following reasons.

Applicant argued that Brown does not disclose "forming a single conducting layer on the at least one metal containing barrier layer", "metal containing spacers beginning at a lower surface of said at least one metal containing barrier layer and extending substantially to an upper surface of said second dielectric layer", "said single conducting layer comprising at least copper or aluminum and comprising an upper surface, said upper surface of said single conducting layer out of contact with any metal", and "conductive on at least one metal containing barrier layer..second dielectric layer on the conductive layer". The examiner disagreed, Brown discloses all of the features indicated above. First of all, the use of "comprising" in all the independent claims 1, 72, 103, and 106 allow for the existence of additional layers including other conducting layers, therefore even with the limitation "single conducting layer" the claims do not preclude the the presence of additional conducting layer such as layer 14 as disclosed in Brown (see Fig. 4). Applicants appeared to argued that the claims require the (single) conducting layer to be directly formed on the barrier layer. The examiner disagreed, nothing in the claims require such an interpretation, the use of "on" does not require the meaning of "directly on". Therefore the presence of layers 14 and 16 between the metal containing barrier layer 12 and the single

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conducting layer 18 is allowed. In Brown, a second dielectric layer is in contact with the single conducting layer, in Fig. 3, when layer 18 of copper is considered to be the single conducting layer then the oxide layer substituting the layer 20 (see col. 4, lines 40-62) is equivalent to the claimed second dielectric layer and it is in contact with the single conducting layer 18. Note that when a silicon oxide layer is used instead of an ARC layer, the upper surface of the single conducting layer 18 is out of contact with any metal. Fig. 3 in Brown clearly shows that the spacers 22 of TiN or TaN beginning at a lower surface of said at least one metal containing barrier layer 12 and extending substantially to an upper surface of said second dielectric layer (when the ARC layer 20 is substituted by a silicon oxide layer). Therefore Brown does make obvious the limitations of the claims 1-11, 14-26, 72-89, and 92-106.

The response to Applicant's argument concerning the rejection using Liu and Brenna will be incorporated in the modified ground of rejection given below.

### ***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1-11, 14-26, 72-82, 84-89, and 92-106 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown (U. S. Patent 6030896).

[Claims 1 and 72-74] Referring to Figs. 1-5 and related text, Brown discloses a method of fabricating a semiconductor device, comprising the steps of: forming a substantially planar first dielectric layer 10 on a substrate (see col. 4, lines 11-13); forming at least one metal containing barrier layer 12 over the first dielectric layer; forming a single conducting layer 18 over the at least one metal containing barrier layer; forming a second dielectric layer in contact with the single conducting layer (see col. 4, lines 50-62); removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing barrier layer to form a

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multilayer structure (see Fig. 2); and forming metal containing spacers 22 on sidewalls of the multilayer structure, said metal containing spacers being substantially the same height as said multilayer structure (see Fig. 3), for claim 72, the corresponding single conducting layer is 16 and the spacer 22 extending to substantially the same height as said single conducting layer. But it does not disclose expressly that the spacer is of a metal containing material. However, the missing limitation is well known in the art because Brown also discloses that Ta, Ti, TaN, and TiN are equivalently used diffusion barrier material (See col. 4, lines 15-19).

[Claims 2 and 78] wherein said forming the first dielectric layer comprises forming a silicon oxide or BPSG layer (see col. 4, lines 11-14);

[Claims 3, 5, 79, and 80] wherein said forming the at least one metal containing layer comprises forming the at least one metal layer of Ti, Ta, W, Co or Mo or an alloy or a compound of any thereof, including TaN or TiN and wherein said forming the at least one metal containing layer comprises forming the at least one metal layer of titanium or titanium nitride (see col. 4, lines 15-18);

[Claims 4 and 81] comprising forming a metal containing barrier layer 12, said metal containing layer comprising TiN, TiW, WN, or TaN (see col. 4, lines 13-19), the examiner takes official notice that it is well known in the art that Ti and TaN are conventionally used in combination with TiN and TaN, respectively, to increase adhesion, in this case a second metal containing barrier layer is between a first metal containing barrier layer of said at least one metal containing barrier layer and the substrate

[Claims 6 and 82] wherein said forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer of titanium or titanium nitride (see col. 4, lines 13-19);

[Claim 7] in the case where the etch stop layer 16 is of SiN, a conventional etch stop layer, single conducting layer 14 comprises forming the conducting layer from at least one of aluminum and copper (see col. 4, lines 32-49) and the second dielectric layer would be SiN 16;

[Claims 8 and 84] Brown does not teach wherein said forming the single conducting layer comprises forming the conducting layer of an aluminum-copper alloy. However the examiner takes Official Notice that aluminum-copper is a conventional conducting material used in semiconductor device when lower cost and ease of fabrication are desirable.

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[Claims 9, 10, 85 and 86] wherein said forming the metal containing spacers comprises forming at least one layer of Ti, Ta, W, Co or Mo, or alloys thereof or compounds thereof, including TaN and TiN ; wherein said forming the metal containing spacers comprises forming the metal containing spacers of titanium or titanium nitride (see col. 4, line 11-col. 5, line 5);

[Claims 11 and 89] wherein said forming a second dielectric layer comprises forming the second dielectric layer on the single conducting layer to have sidewalls aligned with sidewalls of the conducting layer, and forming the metal containing spacers to extend along the sidewalls of the second dielectric layer (see Fig. 2 and col. 4, lines 50-62);

[Claims 14 and 92] further comprising forming the at least one metal containing barrier layer and the metal containing spacers of a same metal, in the case where the layer 12 is formed of TiN or TiN (see col. 4, lines 15-18 and 63-67);

[Claims 15-18, and 93-96] Brown discloses substantially the limitations of claims 15-18, and 93-96, as shown above. But Brown does not disclose the method of deposition the at least one metal containing barrier layer and the single conducting layer. However, it would have been obvious for a person of ordinary skill in the art to use CVD to deposit the layers to have the same method of deposition as the metal containing spacer layers to obtain conformal layers and to reduce the equipment requirements (see par. bridging cols. 4 and 5);

[Claims 19, 20, 97, and 98] wherein said forming the metal containing spacers comprises forming the metal containing spacers by CVD, vapor deposition and directional etching (see par. bridging cols. 4 and 5);

[Claims 21 and 99] wherein removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing barrier layer to form a multilayer structure is effected by patterning and etching the second dielectric layer, single conducting layer, and at least one metal containing barrier layer (see col. 4, lines 50-62);

[Claims 22-24, 88, 100-103, and 105] wherein said forming the metal containing spacers comprises forming the metal containing spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first and second dielectric layers; wherein said forming the metal containing spacers comprises forming the metal containing spacer layer over the multilayer structure and first dielectric layer by conformal deposition

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process; wherein portions of the metal containing spacer layer over the multilayer structure and first dielectric layer are removed by etching (See par. bridging cols. 4 and 5);

[Claims 75 and 87]wherein flanking at least one surface of the multilayer structure with a metal spacer comprises forming a metal containing spacer 22 layer on said second dielectric layer or on sidewalls of said multilayer structure (see Figs. 3, 5 and par. bridging cols. 4 and 5);

[Claims 25, 26, 76, 77, 104, and 106]further comprising removing any remaining portion of the second dielectric layer and upper portions of the metal spacers laterally adjacent thereto (see Fig. 5); by etching (see col. 5, lines 18-33 ).

Therefore, it would have been obvious to use Brown's teaching to obtain the invention as specified in claims 1-11, 14-26, 72-82, 84-89, and 92-106.

5. Claims 12, 13, 90, and 91 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brown in view of Liu et al. (USPN 6277745, hereinafter "Liu").

Brown discloses substantially the limitations of claims 12, 13, 90, and 91, as shown above.

But it does not disclose expressly the second dielectric layer of a low dielectric constant material, of fluorine-doped silicon oxide.

However, the missing limitations are well known in the art because Liu discloses forming the second dielectric layer of polyimide, a low dielectric constant material (see col. 5, lines 1-5). Liu also discloses that polyimide and SiO<sub>2</sub> are equivalently used for the second dielectric layer. The combined teaching of Brown and Liu does not disclose expressly that the second dielectric layer is of fluorine-doped silicon oxide. However, the examiner takes Official Notice that it is well known in the art that polyimide and fluorine-doped silicon oxide are low k alternatives used in the fabrication of a semiconductive device.

A person of ordinary skill is motivated to modify Brown with Liu to reduce capacitance of the device ensuring faster device.

Therefore, it would have been obvious to combine Brown with Liu to obtain the invention as specified in claims 12, 13, 90, and 91.

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6. Claims 1, 11-13, 72-75, and 88-91 are rejected under 35 U.S.C. 103(a) as being unpatentable over Liu et al., U. S. Patent 6277745 (Hereinafter Liu).

[Claims 1, 72-75, and 88] Referring to Figs. 2A-2F and related text, Liu discloses a method for making a metallization structure for a semiconductor device, comprising: forming a substantially planar first dielectric layer 2 (see col. 3, lines 31-35); forming at least one metal containing barrier layer 4 over the first dielectric layer; forming a single conducting layer 6, 8 on the at least one metal containing barrier layer, said single conducting layer comprising at least Cu or Al and comprising an upper surface, said upper surface of said single conducting layer out of contact with any metal, note that the claims do not require the single conducting layer to be homogeneous; forming a second dielectric layer 16 over the single conducting layer; removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing barrier layer to form a multilayer structure (see Fig. 2B); and forming metal containing spacers on sidewalls of the multilayer structure, said metal spacers beginning at a lower surface of said at least one metal containing barrier layer and extending substantially to an upper surface of said second dielectric layer (see Fig. 2D); wherein flanking at least one surface of the multilayer structure with a metal spacer comprises forming a metal containing spacer 12 layer on said second dielectric layer (see Fig. 2C and col. 4, lines 20-67). The height of the spacer depends on the duration of the etching, when the etching is longer the spacer would be extending to substantially the same height as the conducting layer. But it does not disclose expressly that the first dielectric layer is formed on a substrate. However, the examiner takes Official Notice that it is well known in the art that a dielectric layer is formed on a substrate.

[Claims 11 and 89] Liu also discloses wherein said forming a second dielectric layer comprises forming the second dielectric layer on the single conducting layer to have sidewalls aligned with sidewalls of the conducting layer (see Fig. 2B), and forming the metal spacers to extend along the sidewalls of the second dielectric layer (see Fig. 2D); and

[Claims 12 and 90]; further comprising forming the second dielectric layer of a low dielectric constant material (see col. 5, lines 1-5).

[Claims 13 and 91] Liu discloses substantially the limitations of claims 13 and 91, as shown above. But it does not disclose expressly that the second dielectric layer is of fluorine-doped silicon oxide. However, the examiner takes Official Notice that it is well known in the art

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that polyimide and fluorine-doped silicon oxide are low k alternatives used in the fabrication of a semiconductive device .

Therefore, it would have been obvious to use Liu' s teaching to obtain the invention as specified in claims 1, 11-13, 72-75, and 88-91.

7. Claims 1-12 and 14-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Brenna et al. ( U.S. Patent 6074943, hereinafter "Brenna") .

[Claims 1-3, 5-11, 14, and 19-24] Referring to 2A-2H and related text, Brenna discloses a method for making a metallization structure for a semiconductor device, comprising: forming a first dielectric layer 200 of silicon oxide; forming at least one metal containing barrier layer 205 of TiN, over the first dielectric layer (see col. 2, lines 37-42); forming a single conducting layer 210, 215 over the at least one metal containing layer, note that the claims do not require the single conducting layer to be homogeneous; forming a second dielectric layer 220 over the single conducting layer; removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing barrier layer to form a multilayer structure (see Fig. 2D); and forming metal containing spacers 240 of TiN on sidewalls of the multilayer structure, said metal spacers begining at a lower surface of said at least one metal containing barrier layer and extending substantially to an upper surface of said second dielectric layer (see Fig. 2F and col. 3, lines 28-34, col. 4, lines 32-58). But it does not disclose expressly that the first dielectric layer is formed on a substrate and it is substantially planar dielectric. However, the examiner takes Official Notice that in a semiconductor device it is well known in the art that a dielectric layer is formed on a semiconductor substrate.

[Claim 4] the barrier layer 205 is a metal containing barrier layer of TiN, the examiner takes official notice that it is well known in the art that Ti is conventionally used in combination with TiN, to increase adhesion, in this case a second metal containing barrier layer is between a first metal containing barrier layer of said at least one metal containing barrier layer and the substrate;

[Claim 12] Forming second dielectric layer of low dielectric constant (see col. 6, lines 33-39).

[Claims 15-18] Brenna discloses substantially the limitations of claims 15-18, as shown above. But Brenna does not disclose the method of deposition the at least one metal containing barrier layer and the single conducting layer. However, it would have been obvious for a person of ordinary skill in the art to use CVD to deposit the layers to have the same method of deposition as the metal containing spacer layers to obtain conformal layers and to reduce the equipment requirements (see par. bridging col. 2, lines 51-58).

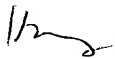
Therefore, it would have been obvious to use the teaching of Brenna to obtain the invention as specified in claims 1-12 and 14-24.

### *Conclusion*

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ha Nguyen whose telephone number is (703)308-2706 . The examiner can normally be reached on Monday-Friday from 8:30AM to 6:00PM, except the first Friday of each bi-week.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling, can be reached on (703) 308-3325. The fax phone number for this Group is (703) 308-7722.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956.



Ha Nguyen

Primary Examiner

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